

FIG.1

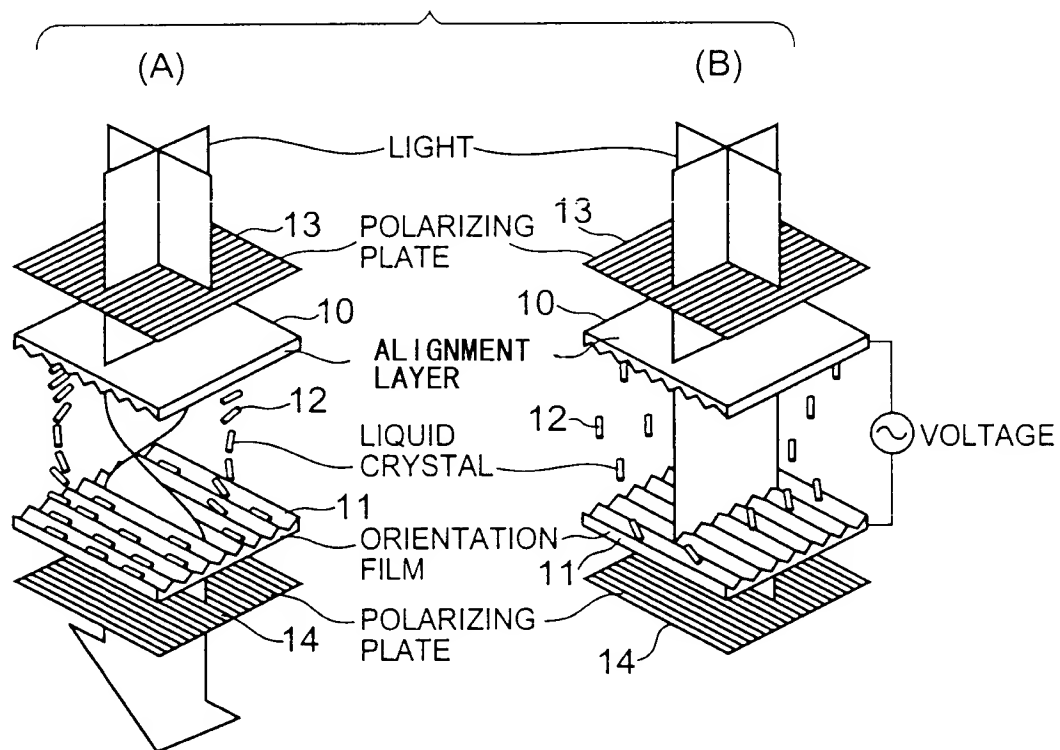


FIG.2

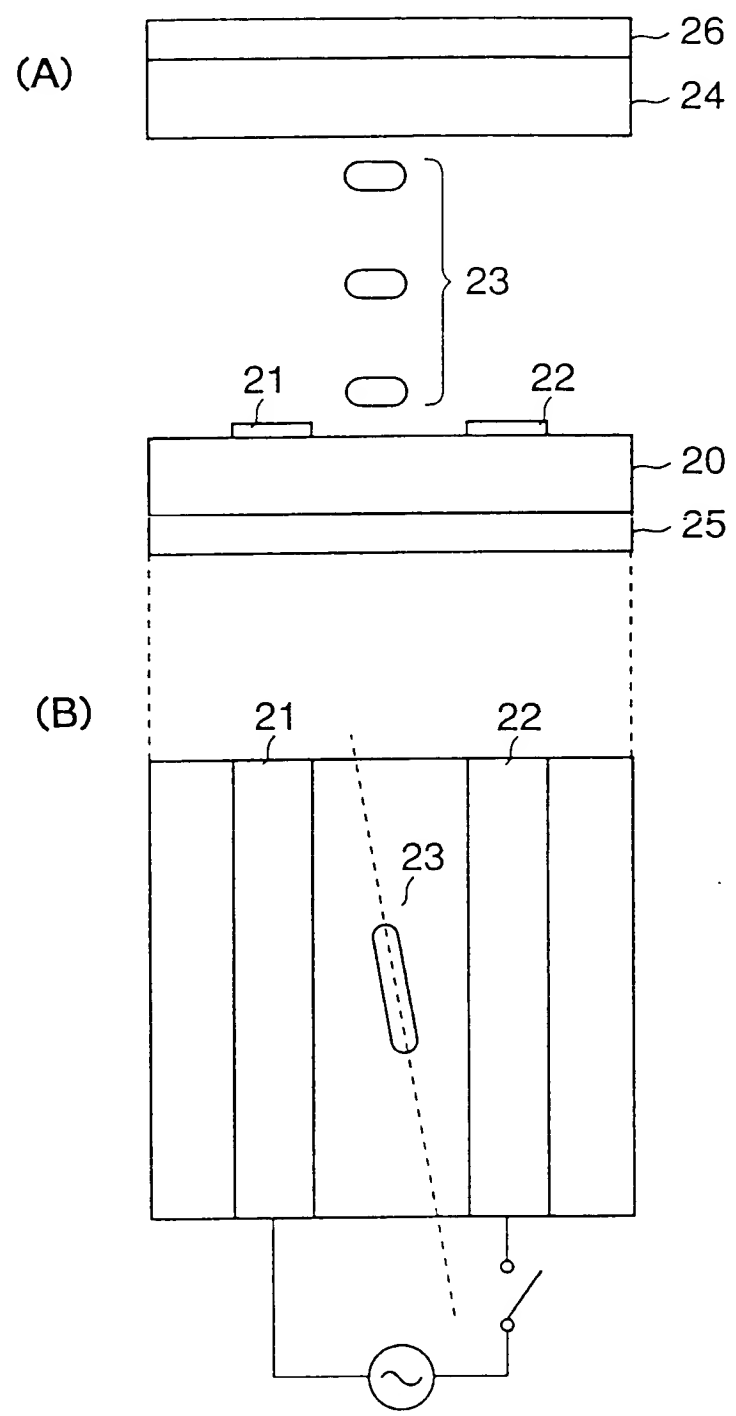


FIG.3

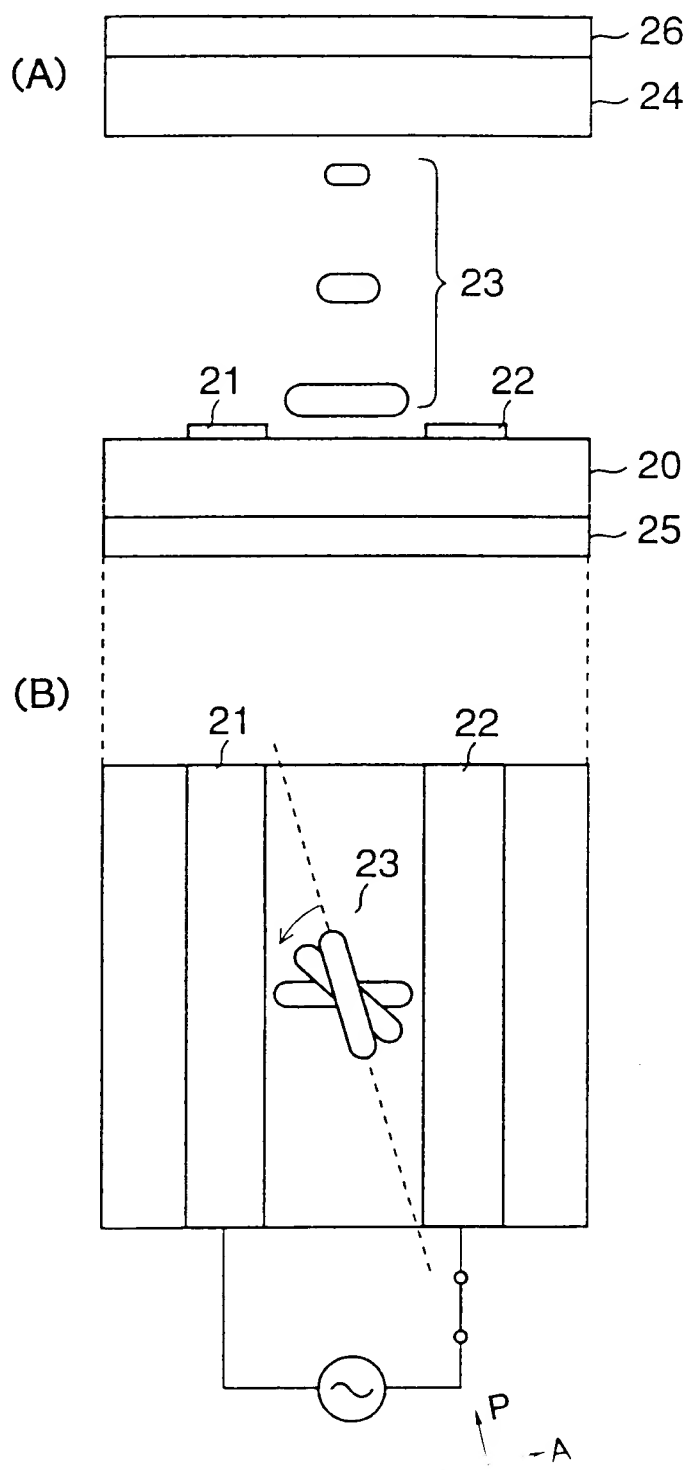


FIG.4

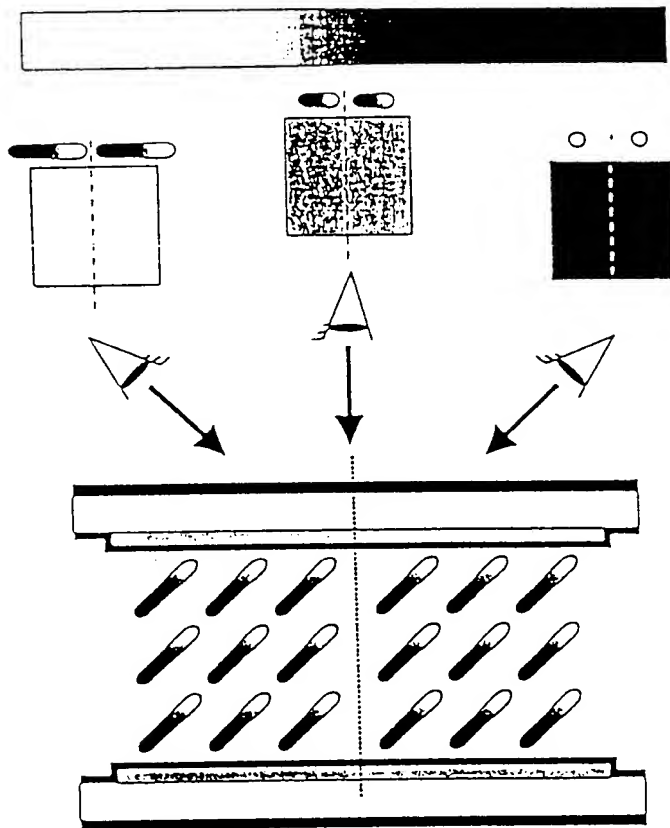


FIG.5

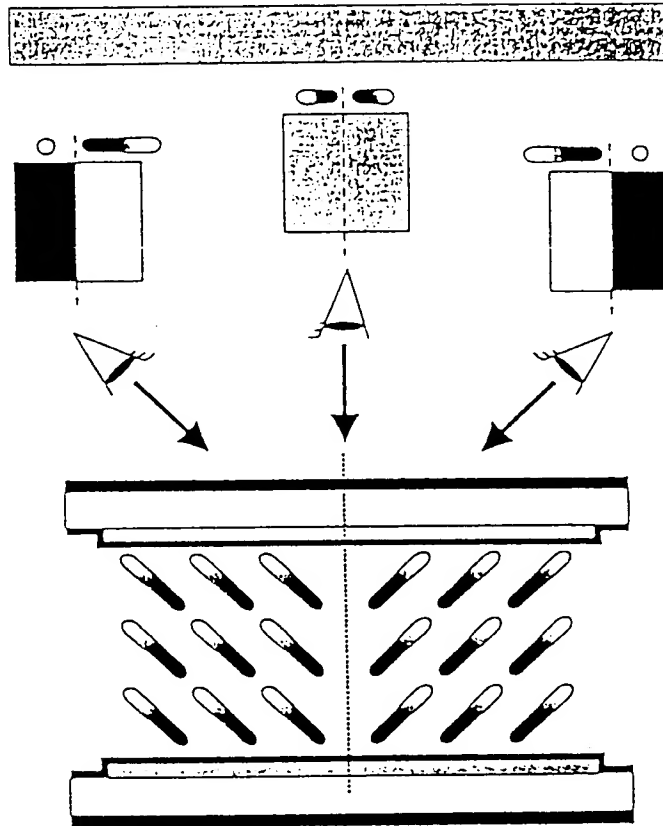
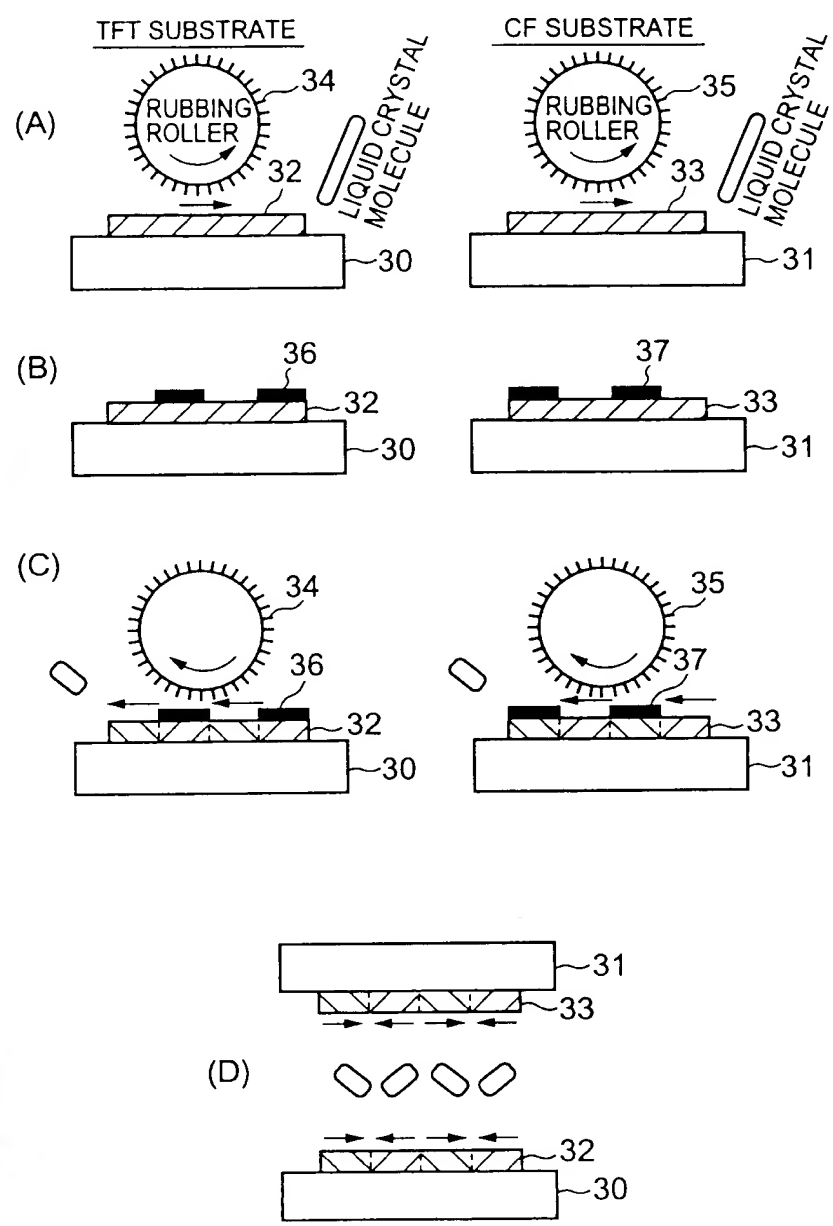


FIG.6



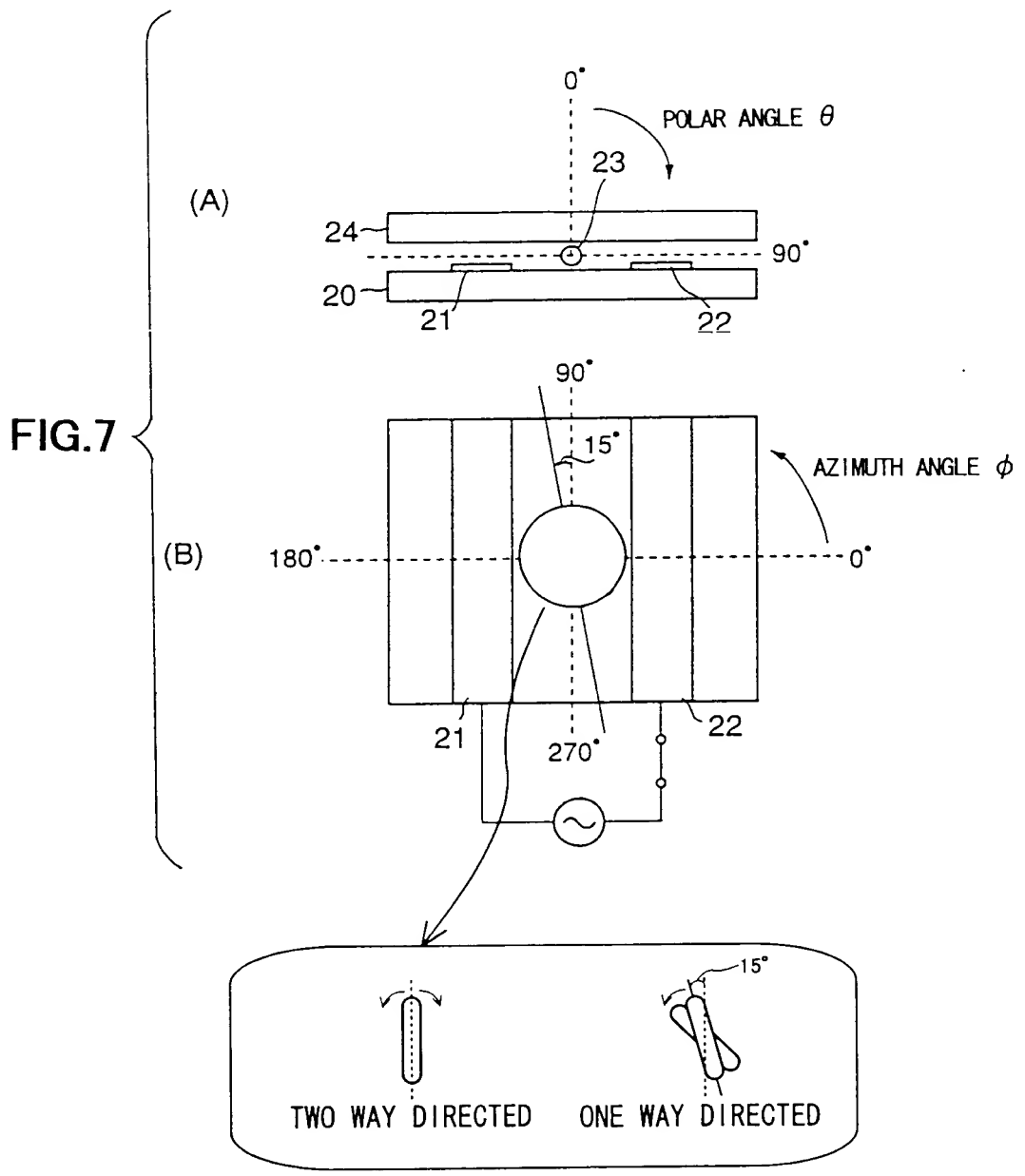


FIG.8

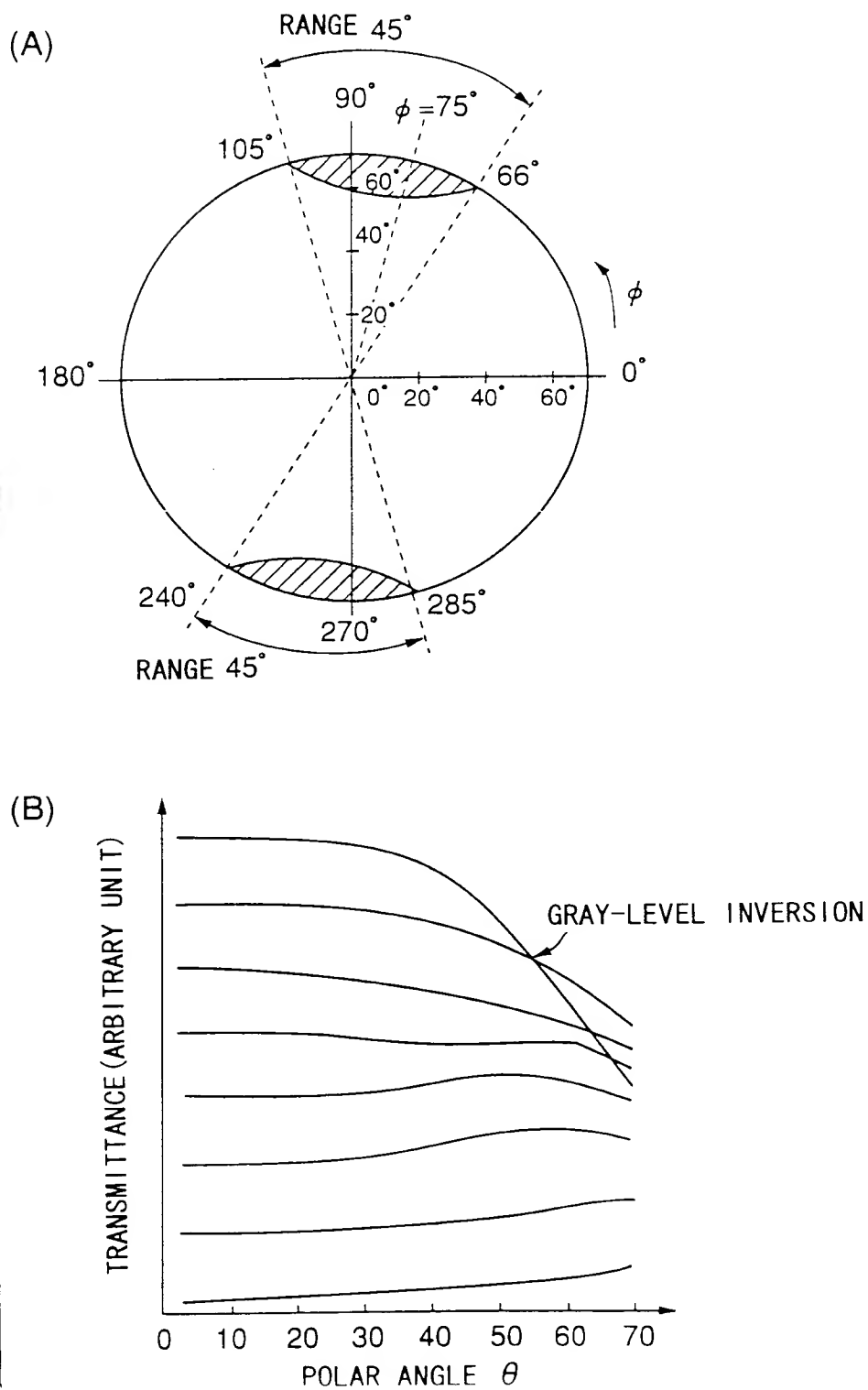




FIG.9

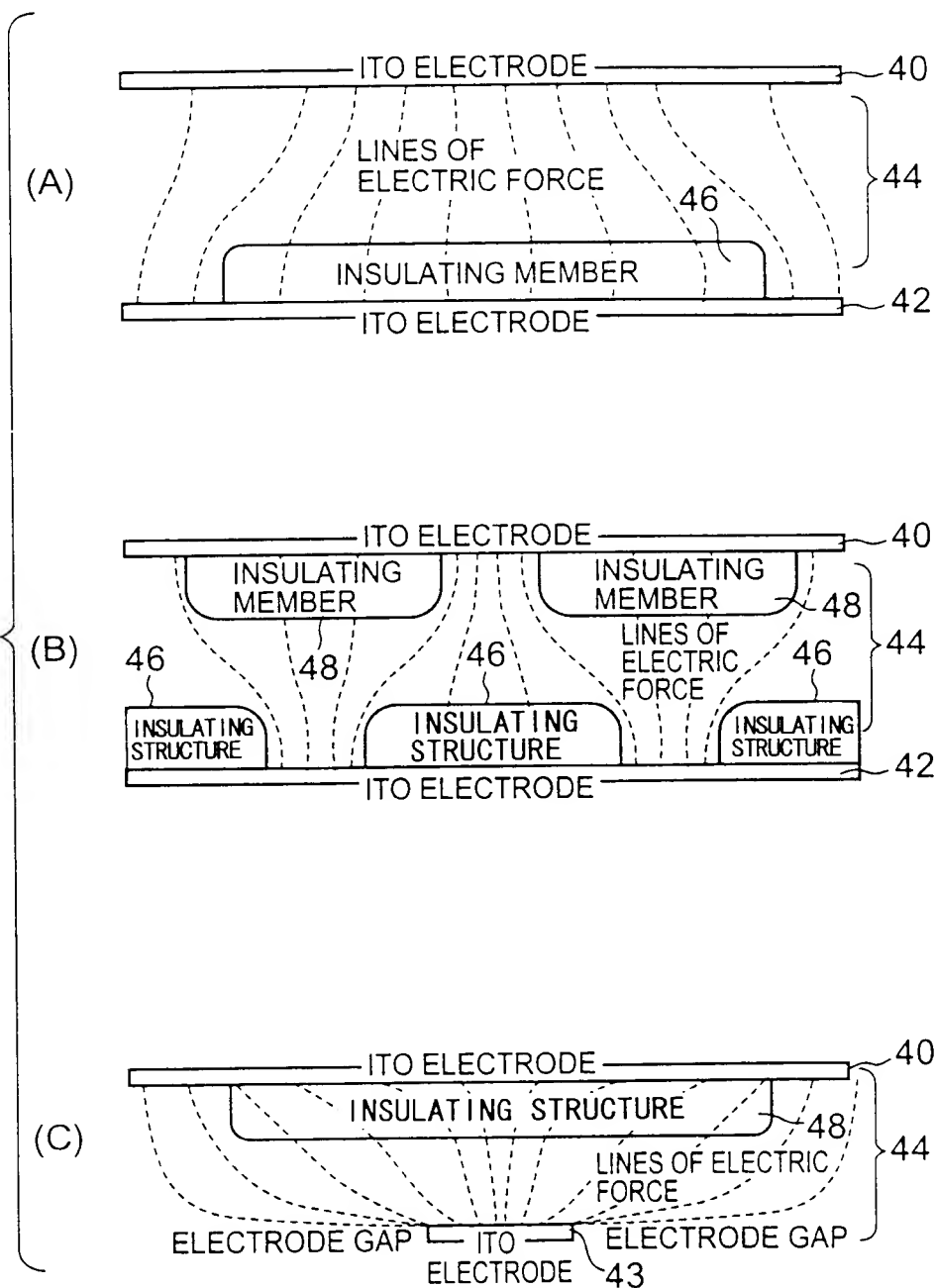


FIG.10

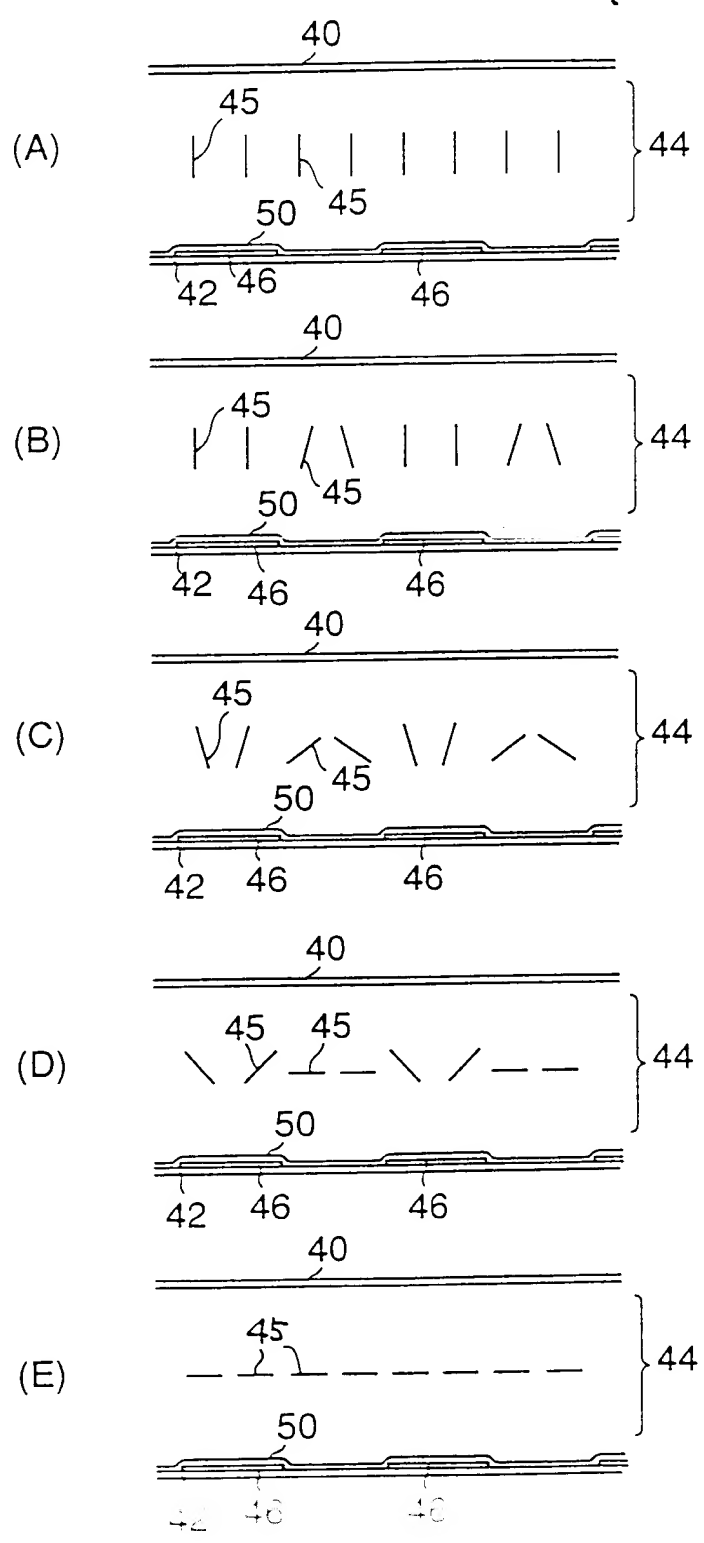


FIG.11

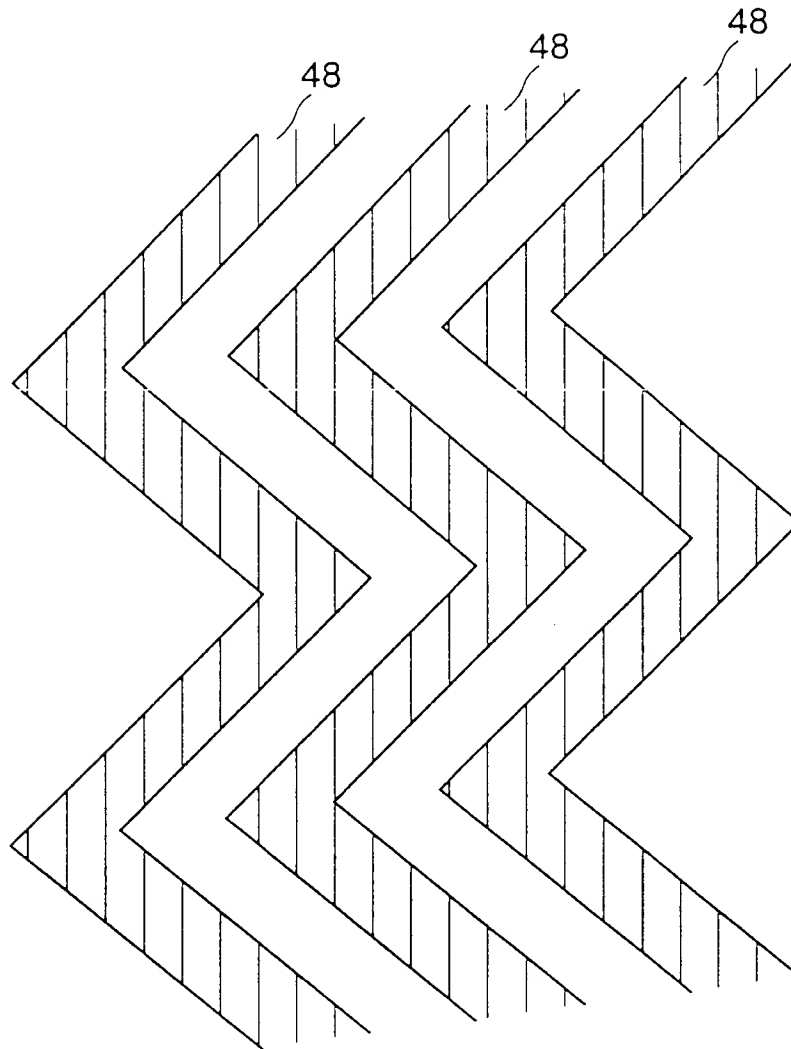


FIG.12

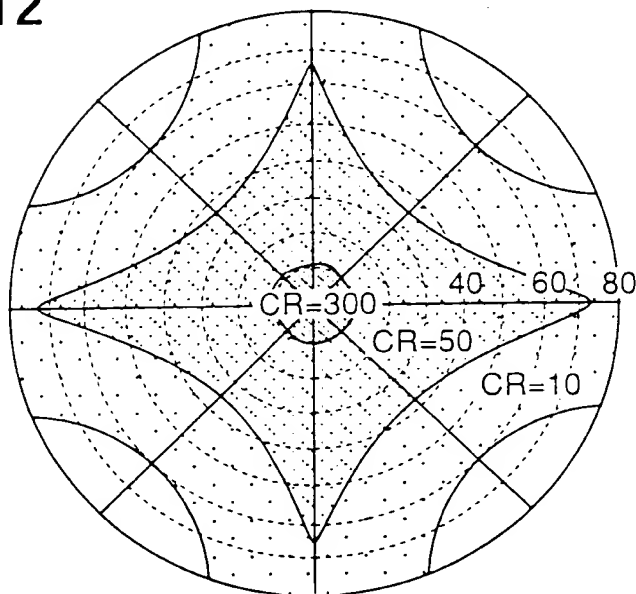


FIG.13

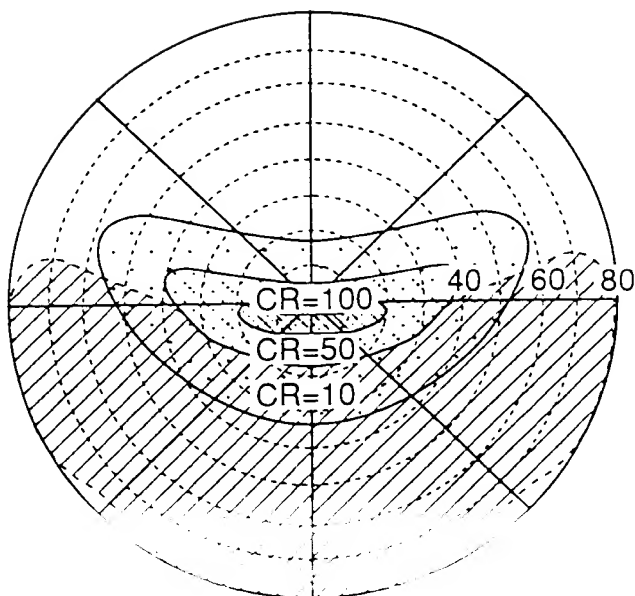


FIG.14

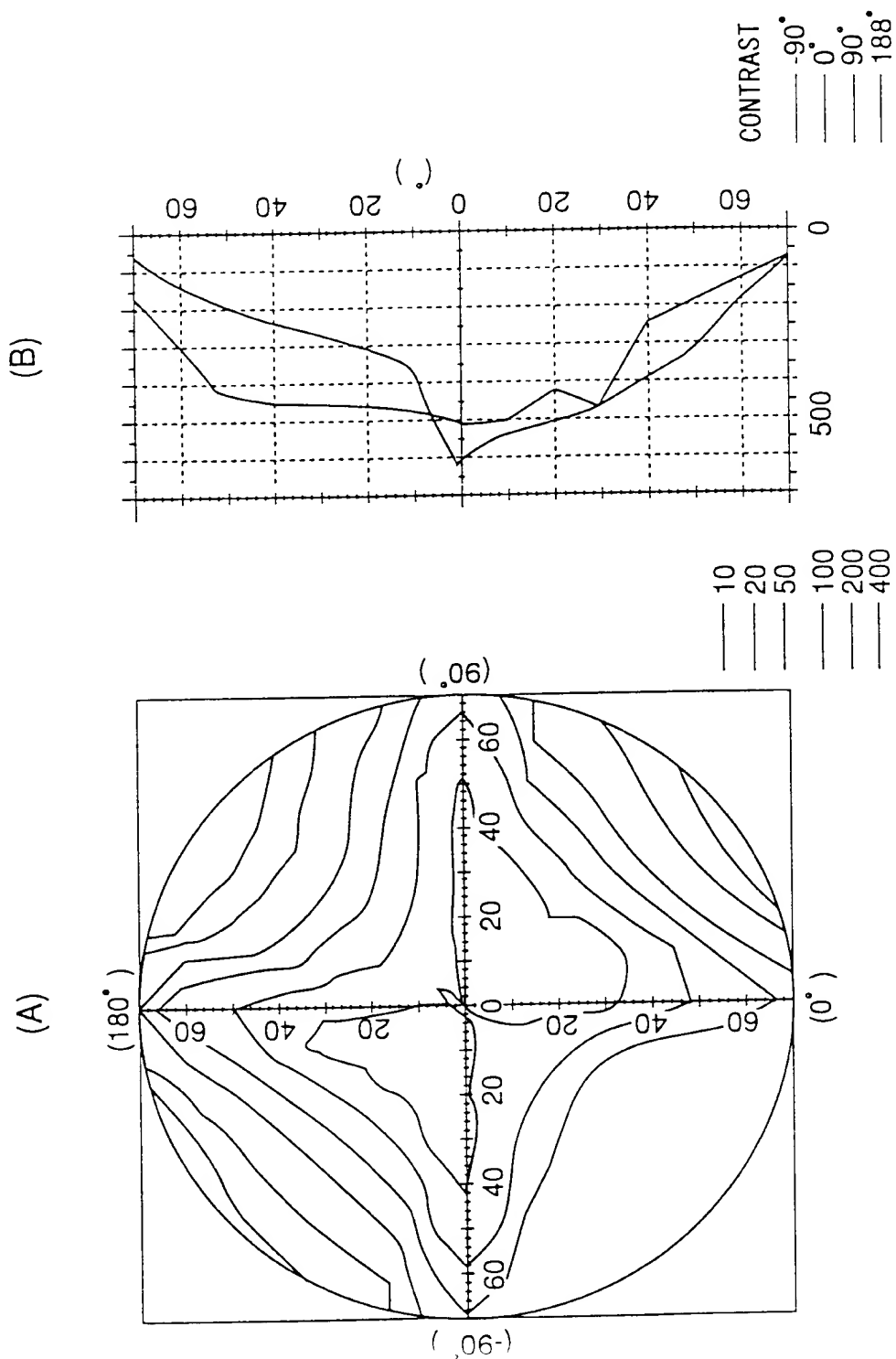
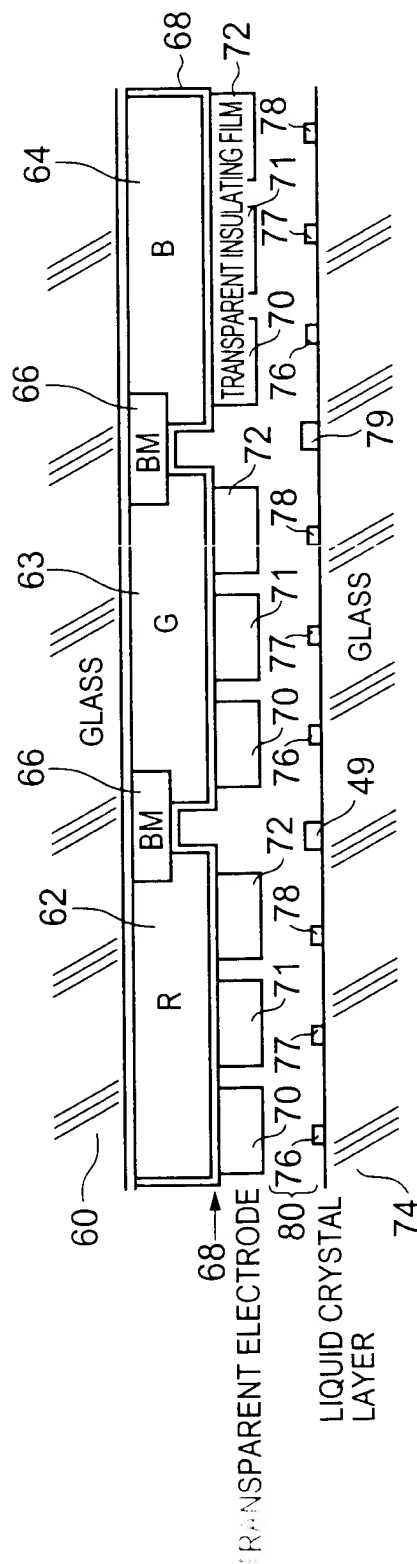


FIG.15



This diagram shows a cross-sectional view of a pixel structure. A horizontal line at the top is labeled "GATE BUS LINE 84". Below this line, three vertical electrodes are labeled 70, 71, and 72. To the left of these electrodes is a structure labeled "TFT 82". The electrodes 70, 71, and 72 are part of a larger structure labeled 68. The area between the electrodes is labeled 76, 77, and 78. A vertical line on the left is labeled "DATA BUS LINE 79".

FIG.17

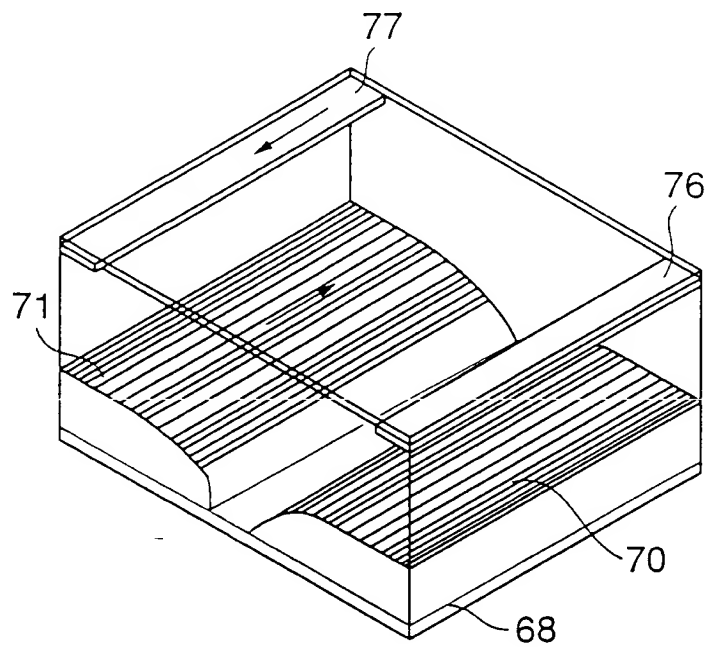






FIG.19

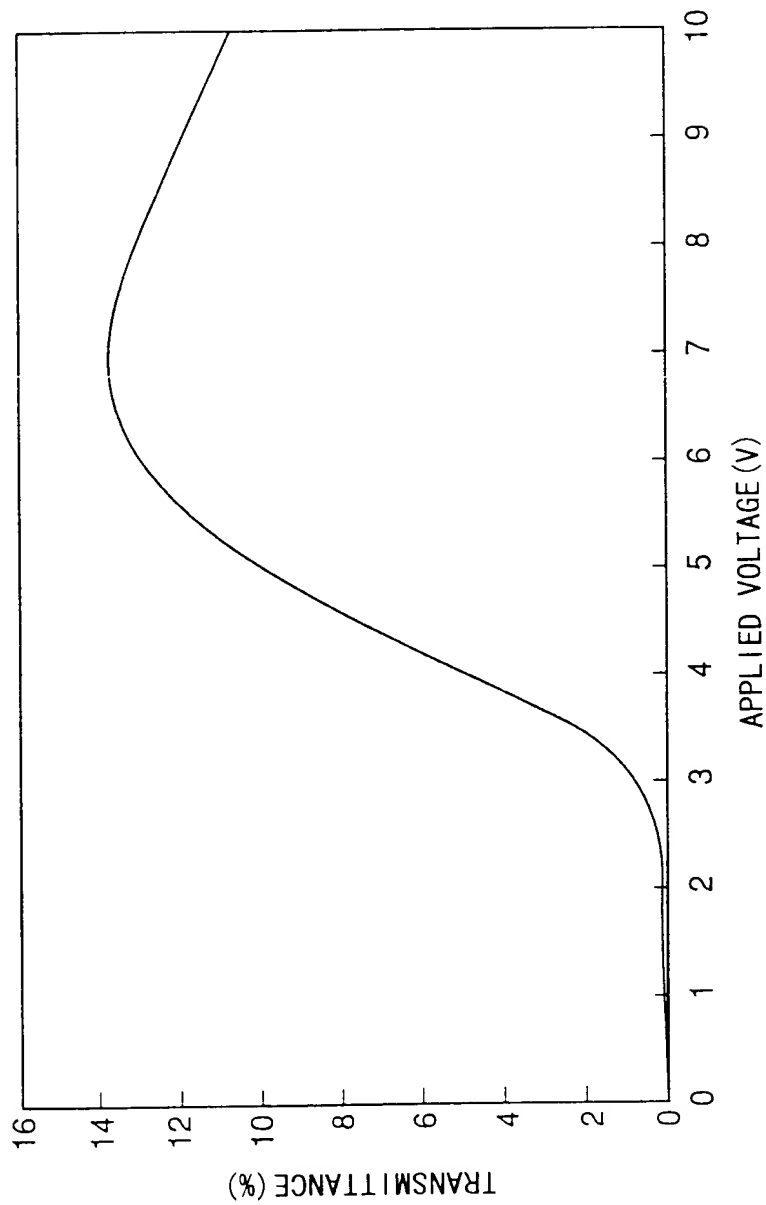
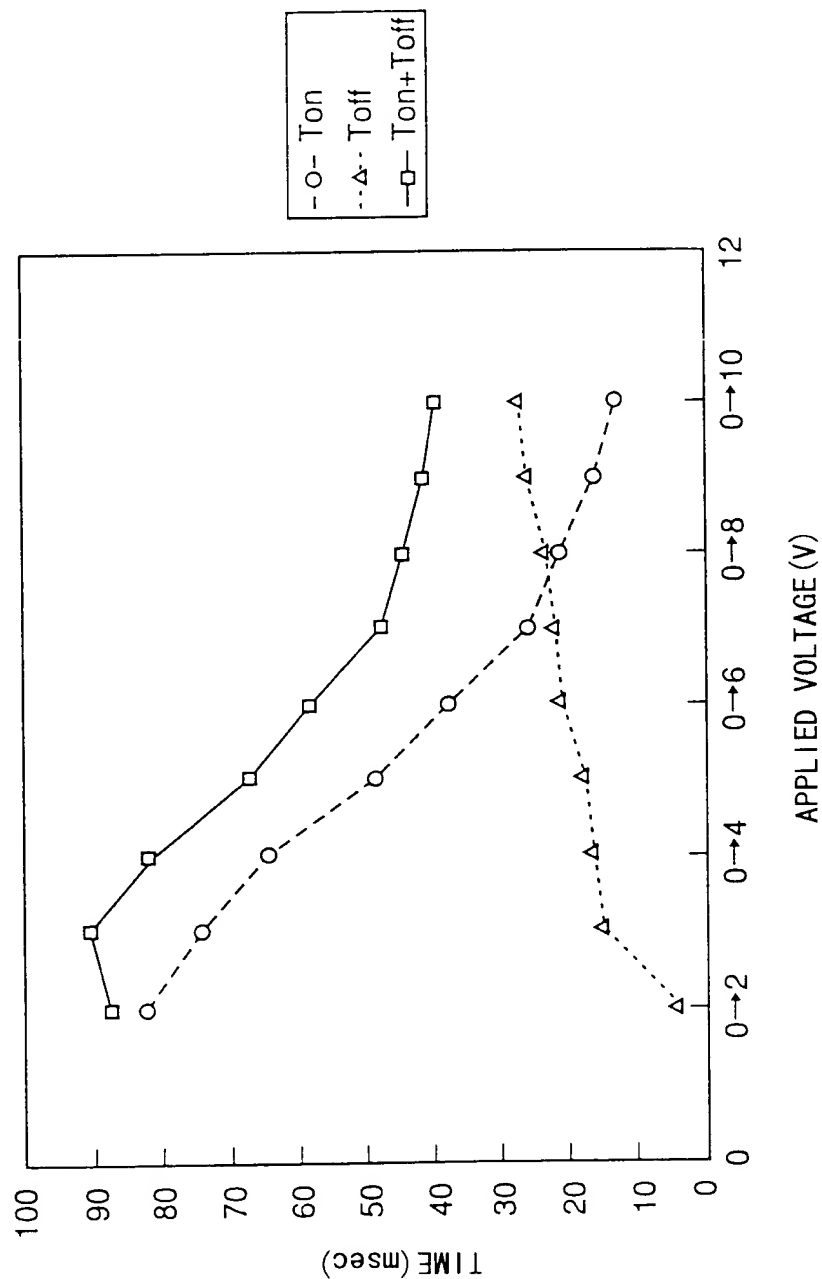
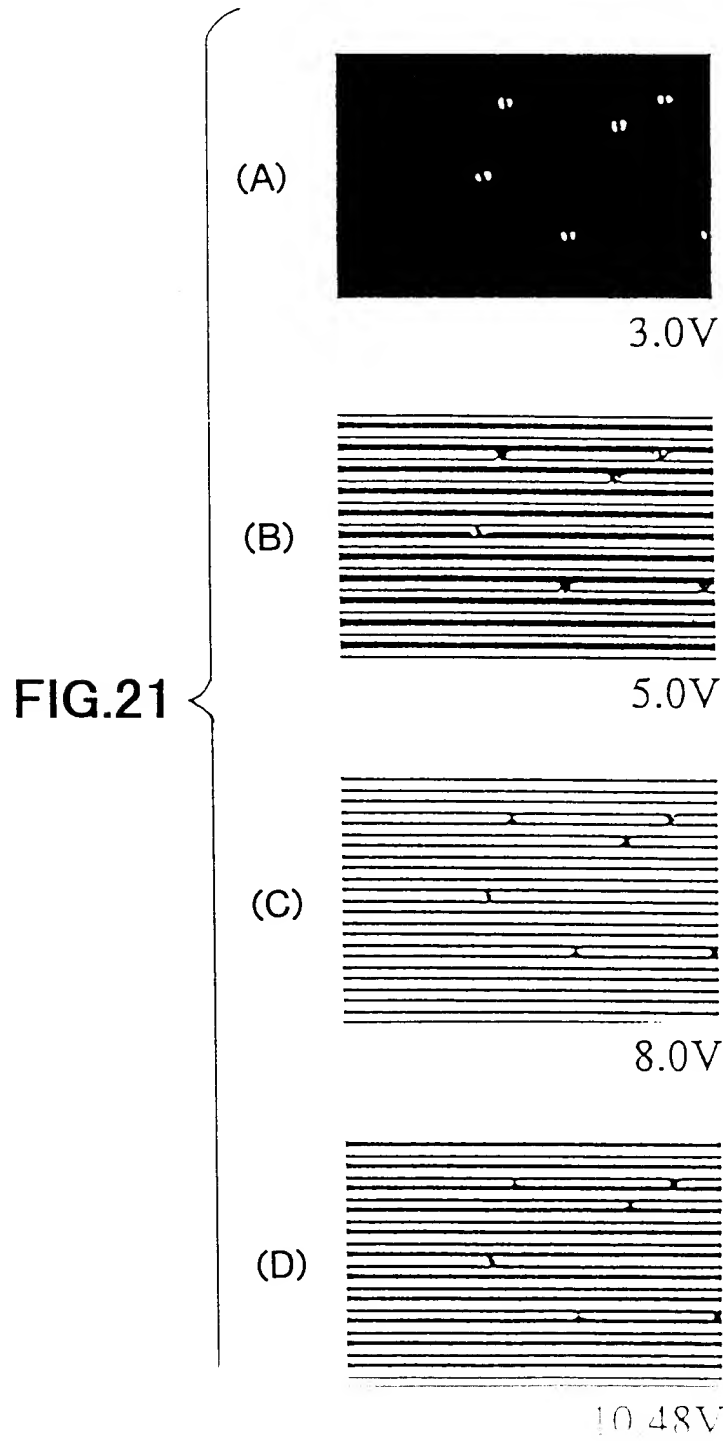
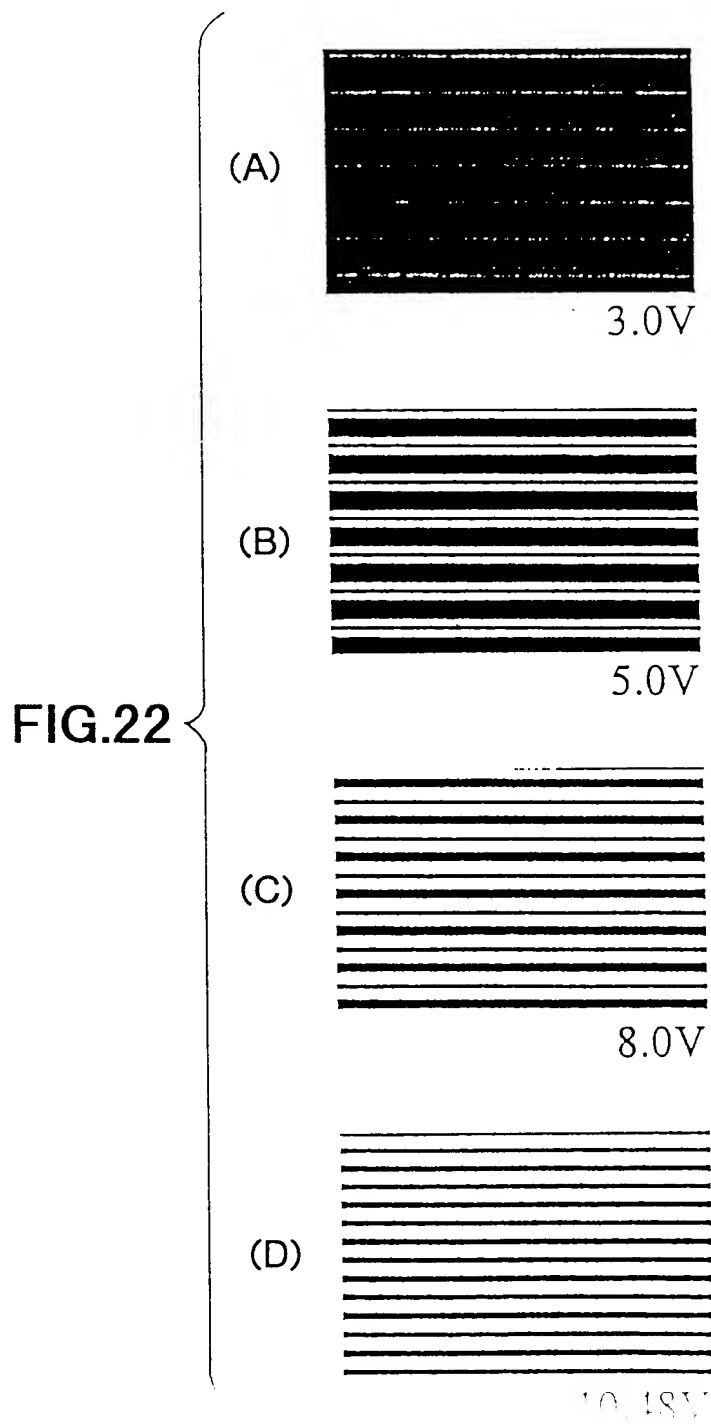


FIG.20







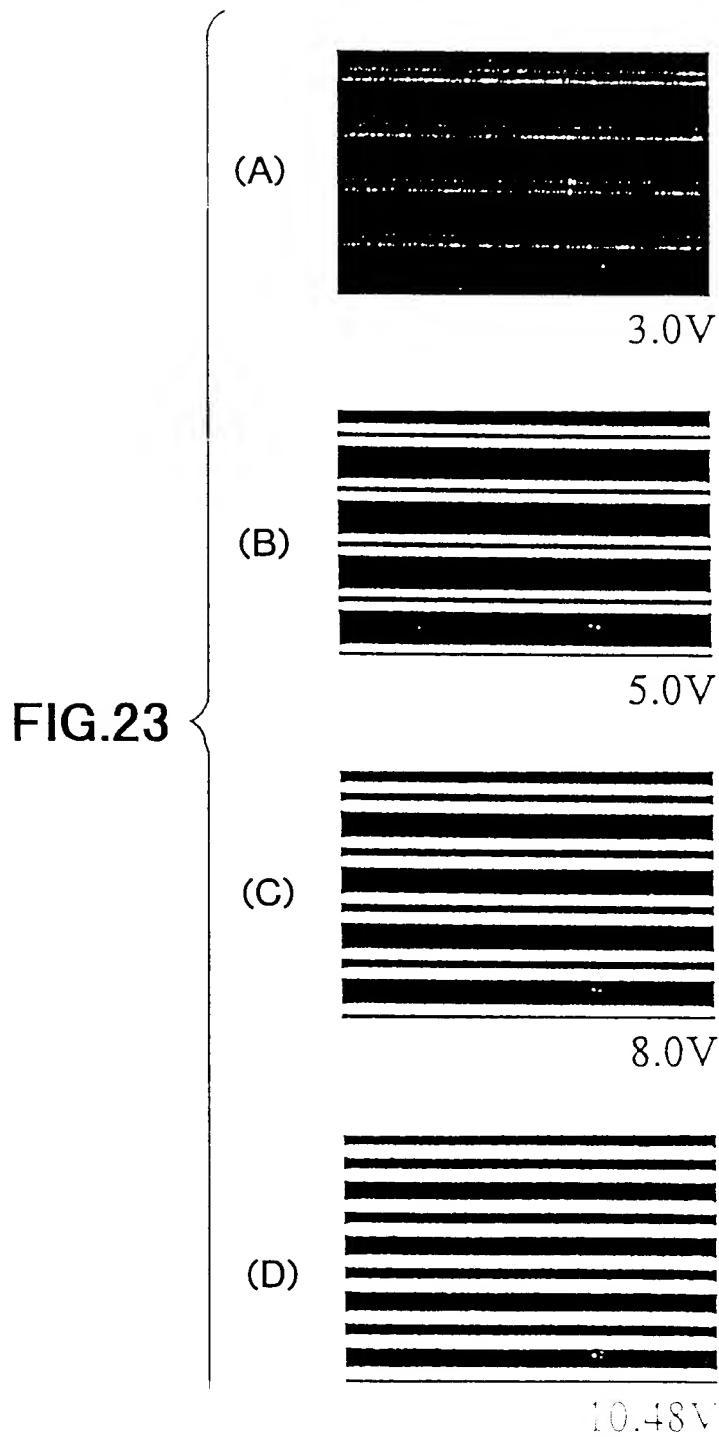


FIG.24

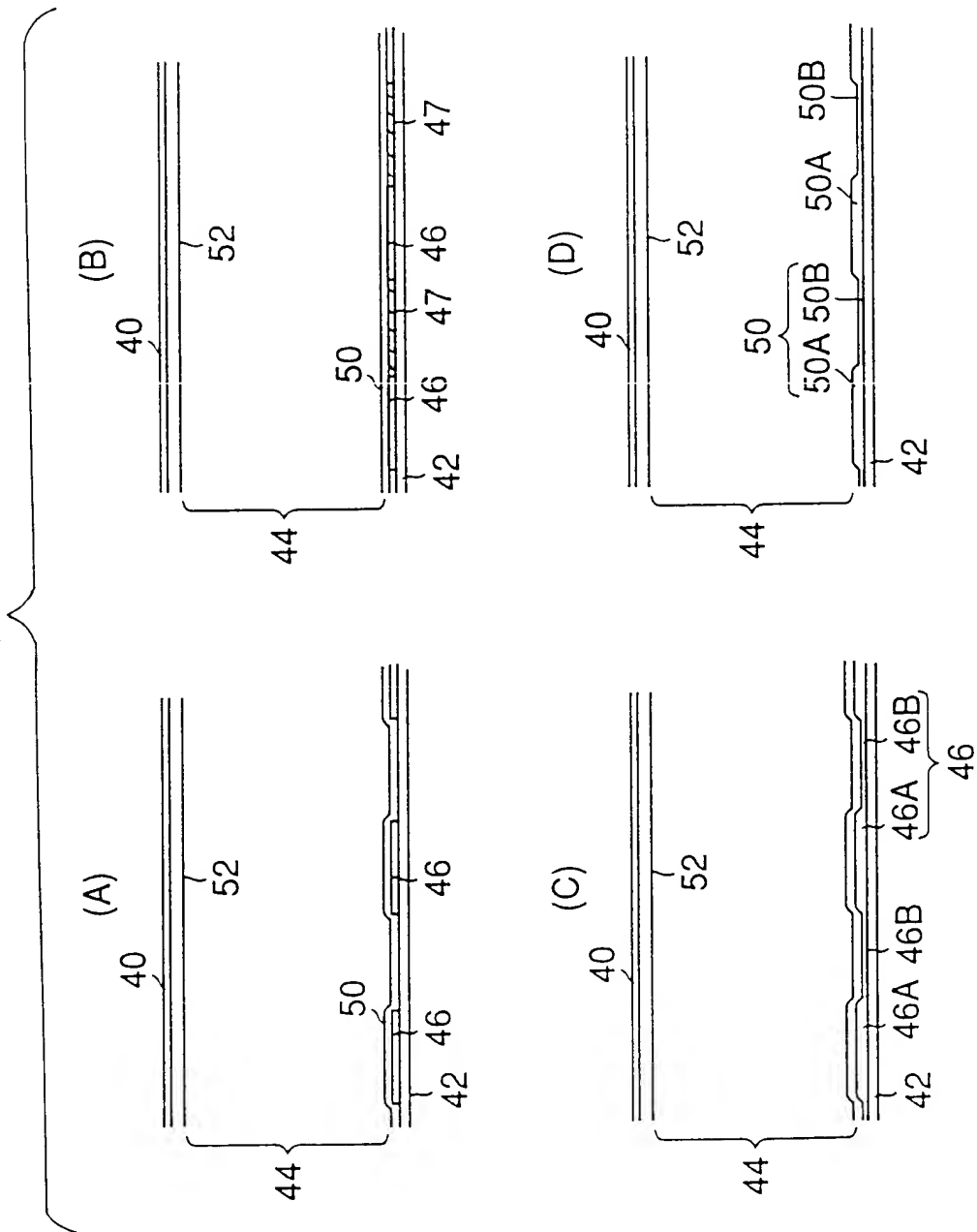


FIG.25

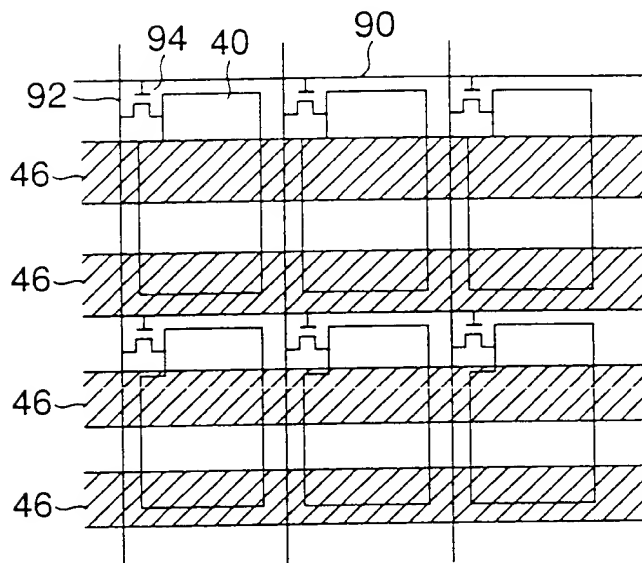




FIG.26

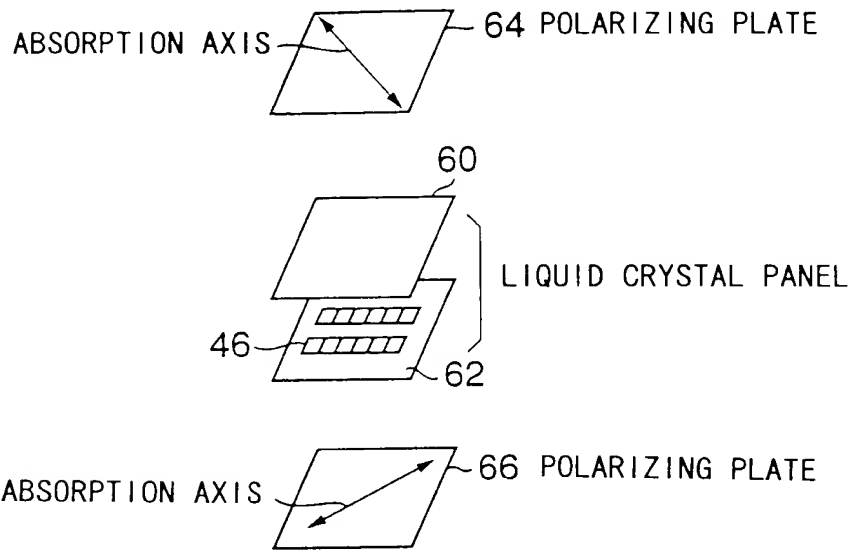


FIG.27

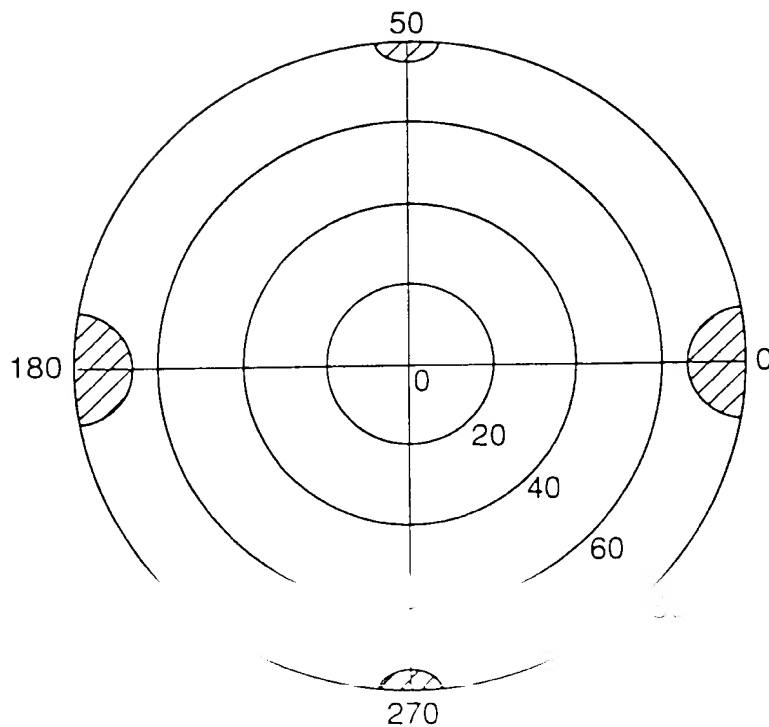


FIG.28

